Programming Texas Instruments Keystone SoCs using OpenMP

OpenMP BoF, SC’14
Eric Stotzer
### High Performance Embedded Computing

<table>
<thead>
<tr>
<th>Category</th>
<th>Examples</th>
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<tbody>
<tr>
<td>DVR / NVR &amp; smart camera</td>
<td>Video and audio infrastructure, high-performance and cloud computing</td>
</tr>
<tr>
<td>Networking</td>
<td>Portable mobile radio, industrial imaging, medical imaging</td>
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<td>Home AVR and automotive audio, analytics, wireless testers</td>
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- **Media processing**: DVR / NVR, NVR, smart camera, video and audio infrastructure, high-performance and cloud computing, home AVR and automotive audio.
- **Computing**: Networking, mission critical systems, medical imaging, portable mobile radio, industrial imaging.
- **Radar & Communication**: Analytics, wireless testers, industrial control.

**Texas Instruments**
TI Keystone Architecture
Keystone I: C6678 SoC

- Eight 8 C66x cores
- Each with 32k L1P, 32k L1D, 512k L2
- 1 to 1.25 GHz
- 320 GMACS
- 160 SP GFLOPS
- 512 KB/Core of local L2
- 4MB Multicore Shared Memory (MSMC)
- Multicore Navigator (8k HW queues) and TeraNet
- Serial-RapidIO, PCIe-II, Ethernet, 1xHyperlink
Energy Efficiency

LINPACK running on C6678 achieves 25.6 Gflops, ~2.1 Gflops/W


Linpack Power Profile

The plot shows the power consumption over time during a single execution of the Linpack benchmark code. Blue shows memory power, green is added power fed to the DSP and red other module consumers stacked atop. The vertical lines denote the timed section of the code. Distinct phases of execution can be seen, for instance the serial back-substitution at the end of the run. A zoom in also reveals the power peaks caused by DMA block copies to and from the main memory.

DSP Linpack Energy Efficiency

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<tbody>
<tr>
<td></td>
<td>GF/s</td>
<td>%</td>
<td>W</td>
<td>W</td>
<td>W</td>
<td>W</td>
<td>MF/J</td>
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<tr>
<td>127</td>
<td>1.3</td>
<td>4</td>
<td>5.95</td>
<td>1.26</td>
<td>6.07</td>
<td>14.08</td>
<td>176</td>
<td>90</td>
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<td>255</td>
<td>2.8</td>
<td>9</td>
<td>4.78</td>
<td>0.99</td>
<td>5.17</td>
<td>10.95</td>
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<td>511</td>
<td>6.0</td>
<td>19</td>
<td>6.40</td>
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<td>6.58</td>
<td>14.09</td>
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<tr>
<td>1023</td>
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<td>8.02</td>
<td>1.19</td>
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<td>672</td>
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<td>16.9</td>
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<td>1.10</td>
<td>8.13</td>
<td>18.40</td>
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<td>920</td>
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<tr>
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<td>9.20</td>
<td>21.39</td>
<td>2097</td>
<td>1195</td>
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The table shows the power and energy consumption of the major components of the C6678 DSP EVM. Core refers to the C6678 DSP SoC excluding I/O power. Mem is the DDR3 memory subsystem. The 5-9 watts of “Other” power is to a large part, except for about 1.5 W DC converter losses, consumed by debugging and unused hardware features that would not be present in an HPC server node. Therefore the “Core + Mem” power is a good estimate for the energy efficiency of an HPC server node. The values for small problem sizes show deviations due to various parts of the benchmark not being executed. The outmost loop step size is 128 columns, another breakpoint occurs at 1024.
High Density COTS boards

DSPC-8681 ½ length PCIe card - 54Watts

DSPC-8682 PCIe Full-Length Card - 110Watts

DSPC-8682 ATCA blade 350Watts
Keystone II: 66AK2H12/06 SoC
Available HPC Platforms

Programming Heterogeneous Multicore SoCs

Multicore Navigator

TeraNet

Multicore Memory Controller

Network AccelerationPacs

Packet Accelerator

Security Accelerator

5 port 1GbE Switch

High Speed SERDES

SRO

PCle

HyperLink

GbE

System Elements

Power Mgr

SysMon

Debug

EDMA

EMIF and I/O

16b EMIF

UART x2

SPI x3

I2C x3

USB3

16x16x16x16x66x

HD72 Core x2

HP Moonshot

ProLiant m800

nCore

Brown Dwarf

ProDrive PDAK2H

66AK2H Evaluation Module
Heterogeneous Multicore Programming

- Within a node, OpenCL™ or OpenMP® 4.0 can be used to program heterogeneous compute cores
- Across nodes, MPI is used to partition the application and manage program execution, data transfer and synchronization
```c
// OpenMP Accelerator vector add
// OpenMP for loop parallelization
void ompVectorAdd(int N,
    float *a,
    float *b,
    float *c)
{
    #pragma omp target           \
    map(to:   N, a[0:N], b[0:N]) \
    map(from: c[0:N])
    {
        int i;
        #pragma omp parallel for
        for (i = 0; i < N; i++)
            c[i] = a[i] + b[i];
    }
}
```

**Data movement**
- **to** copies variables from the ARM memory to the DSP memory
- **from** copies variables from the DSP memory to the ARM memory
- TI provides special `alloc` and `free` functions to allocate DSP memory such that copies are not needed

**Calling existing DSP code from the ARM**
- Wrapping existing DSP functions with OpenMP Accelerator code is straightforward
OpenMP Compiler support at TI

• OpenMP 3.0 on C667x (DSP only)
  – BIOS MCSDK 2.1.x

• OpenMP 3.0 + OpenMP 4.0 device constructs
  – HPC MCSDK 3.0.x

• Ongoing development to get to 4.0

• Come by the Texas Instruments Booth 3745 at SC